Fabrication, RF Performance, and Yield of a Combined Limiting Amplifier and Dual-Modulus Prescaler GaAs IC Chip

ARTHUR E. GEISSBERGER, MEMBER, IEEE, ROBERT A. SADLER, MEMBER, IEEE, HAUSILA P. SINGH, SENIOR MEMBER, IEEE, GARY K. LEWIS, MEMBER, IEEE, INDER J. BAHL, SENIOR MEMBER, IEEE, MATTHEW L. BALZAN, MEMBER, IEEE, EDWARD L. GRIFFIN, MEMBER, IEEE, AND MONTE J. DRINKWINE, MEMBER, IEEE

Abstract—**We present production technology details, RF performance, and yield results for an ECL-compatible, *L*-band, limiting dual-modulus (÷10/11) prescaler. This multifunction self-aligned gate (MSAG) process for monolithic integration of analog and digital circuit functions uses refractory self-aligned gate FET technology. When tested with −22 dBm input signal power, one lot of six wafers had a total RF chip yield of 19 percent, with a best-wafer yield of 43 percent. The average operating frequency was 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW).**

I. Introduction

CURRENT gallium arsenide technology normally integrates circuit functions onto separate analog and digital chips, due to the significant differences in the processing technologies required to fabricate each type of chip. However, this requires a hybrid assembly with its attendant cost and its reduced reliability versus a combined analog and digital integrated circuit approach. In addition, low power consumption is always desirable for improved system reliability; therefore either of the above approaches would benefit by employing low-power, enhancement/depletion (E/D) mode, direct-coupled field-effect transistor (FET) logic (DCFL) for its digital circuit functions.

In this work we present a production technology which addresses both issues by allowing the fabrication of combined microwave and E/D digital gallium arsenide integrated circuit (IC) chips. The process is based on refractory self-aligned gate (SAG) technology. It allows for the integration of microwave FET's, E- and D-mode digital FET's, diodes, implanted resistors, metal–insulator–metal (MIM) capacitors, and inductors using two and one-half levels of interconnect metal.

We demonstrate this process by fabricating an ECL-compatible *L*-band limiting amplifier and digital dual-modulus (÷10/11) prescaler (buffered prescaler) integrated circuit chip, which will be used in phase-locked loop and frequency synthesizer circuits. Below we present the details of the fabrication process; the design and RF performance of the analog, digital, and combined circuits; and yield data.

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The authors are with the Gallium Arsenide Technology Center, ITT Corporation, Roanoke, VA 24919-1088.

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II. Fabrication Technology

The combined analog and digital process, which is a melding of the ITT analog [1] and digital [2] processes, is illustrated in Fig. 1. This fully planar process (no gate recessing is employed for FET fabrication) employs selective ion implantation into undoped LEC substrates (Fig. 1(a)). Five selective implants are required, one each for the microwave, D-mode digital, and E-mode digital FET's, a fourth for microwave diodes, and a fifth for resistors. Titanium tungsten nitride (TiWN) is then deposited by reactive sputtering [3]. This material forms the thermally stable gate electrode, and it is patterned into "T-gate" structures by reactive-ion etching using a Ni etch mask defined by liftoff (Fig. 1(b); see Fig. 2(a) for a detailed sketch and Fig. 2(b) for a scanning electron micrograph (SEM) of a T-gate structure).

After the T-gate structures have been defined, the wafer is patterned with photoresist in preparation for the n+ implant (Fig. 1(c)). In particular, a stripe of resist overlaps the T gate on the analog FET's, whereas the digital FET's have no resist stripe (see detailed sketch in Fig. 2(c) and SEM in Fig. 2(d)). This results in the n+ implant for the analog FET being asymmetric: self-aligned to the T gate on the source side, but separated from it on the drain side. Thus the separation between the gate and n+ on the source side is nominally 0.2 μm, which results in low parasitic source resistance; however, the separation between the gate and n+ on the drain side is increased to approximately 1 μm by the resist stripe, which increases the output resistance and the breakdown voltage of the analog FET. Hence, an asymmetric n+ implant is used to

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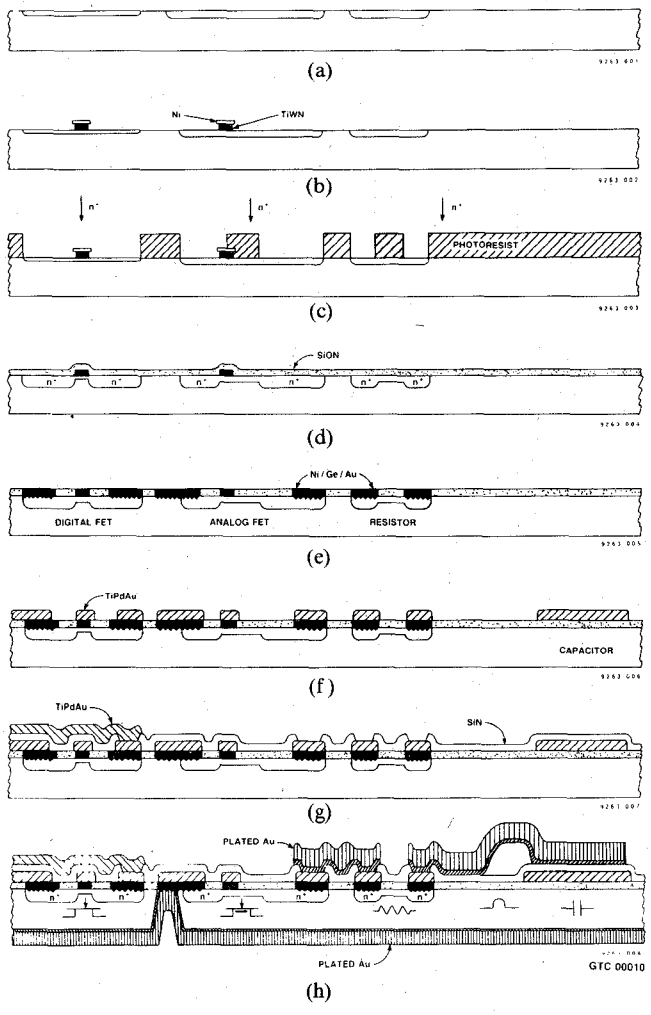


Fig. 1. Combined analog and digital refractory self-aligned gate process flow schematic. (a) Device implants. (b) Gate formation. (c) n^+ implant. (d) Anneal, planarize. (e) Ohmic contacts. (f) First metal. (g) Dielectric, second metal. (h) Plating, backside vias.

improve the analog FET performance, while a symmetric n+ implant for both types of digital FET's results in the best digital performance.

After implant and resist removal, the wafer is capped with plasma-deposited silicon oxynitride (SiON) and annealed to activate all implants (Fig. 1(d)). The SiON is then removed, and plasma CVD silicon nitride (SiN) is deposited and planarized using reflowed resist and a CF_4/O_2 plasma etch-back. This exposes the entire gate electrode for electrical contact by the overlay metal. In addition, using the ohmic-level resist as both a mask for the dielectric-window etch and the liftoff medium, ohmic contact metal is embedded into the planarized dielectric and then alloyed (Fig. 1(e)).

Next Ti/Pd/Au first-level metal is overlaid on the entire width of the gate electrodes (Fig. 1(f)). Since it has both a larger cross-sectional area and a higher electrical conductivity than the underlying TiWN Schottky contact, this overlayer dramatically reduces the gate resistance. Because the Au-based overlayer is insulated from the GaAs surface by the planarizing dielectric, both the alignment tolerance and the linewidth constraint on the overlayer can be relaxed. (This is illustrated by a detailed sketch and an SEM of a finished gate electrode in Fig. 2(e) and (f), respectively.) In addition to reducing the FET gate resistance, this layer overlays the ohmic contact metal to reduce its sheet resistance, forms the bottom plate of MIM capacitors, and serves as first-level interconnect metallization for the entire integrated circuit (Fig. 1(f)).

Silicon nitride, which serves as FET passivation and MIM capacitor dielectric, is deposited and patterned by plasma etching. A layer of polyimide is then added for planarization and is etched off the contact vias and capacitors, and a second level of Ti/Pd/Au interconnect metal is defined by lift-off (Fig. 1(g)). Finally, a third level of plated Au interconnect metal is added to define microwave transmission lines and air bridges for low-capacitance crossovers (Fig. 1(h)). The wafers are then thinned to 125 μm; if required, backside through-vias are etched to the FET source pads using a Ni etch mask, and the backside is plated (Fig. 1(h)). (Backside vias were not used on the circuits in this work.)

III. Circuit Discussion and Results

Since in most military systems analog front ends must eventually interface with digital components, combining analog and digital functions on the same chip can help in reducing the performance degradation which occurs when coupling a signal between them. Therefore, a limiting amplifier and an E/D-mode digital prescaler circuit were combined on a single chip, which will be used in phase-locked loop and frequency synthesizer circuits. Fig. 3 shows circuit schematics and a scanning electron micrograph (SEM) of the buffered prescaler.

In order to facilitate the analysis of the combined circuit performance and yield, the die used for this circuit contained three separate chips: the limiting amplifier, the dual-modulus ($\div 10/11$) prescaler, and the monolithically integrated limiting amplifier and prescaler. The RF performance and yield data that follow were obtained by measuring all three chip types, on one lot of six wafers.

A. Limiting Amplifier

A wide-band six-stage limiting amplifier using feedback was designed. The purpose of the limiting amplifier is to provide a constant output voltage level ($0.4 \pm < 0.4$ V across a 50 Ω load), for a variable input signal power from -30 dBm to -10 dBm, over the 0.2 to 2 GHz frequency range. The analog input signal is essentially converted to a digital signal via the action of the output diode limiters. The minimum linear gain required for the limiting amplifier is about 33 dB.

The operating frequency of the limiting amplifier is 200 MHz to 2.0 GHz. The input stage is a common-gate amplifier which gives a low *VSWR*. Stages two through six provide the amplification needed to convert a low-level input signal to a constant-level output signal. Stages two, four, and six consist of common-source feedback amplifiers and three and five are common-source gain stages. Each amplifier stage is ac coupled (external gate bias has to be supplied to each stage), and the last three stages of

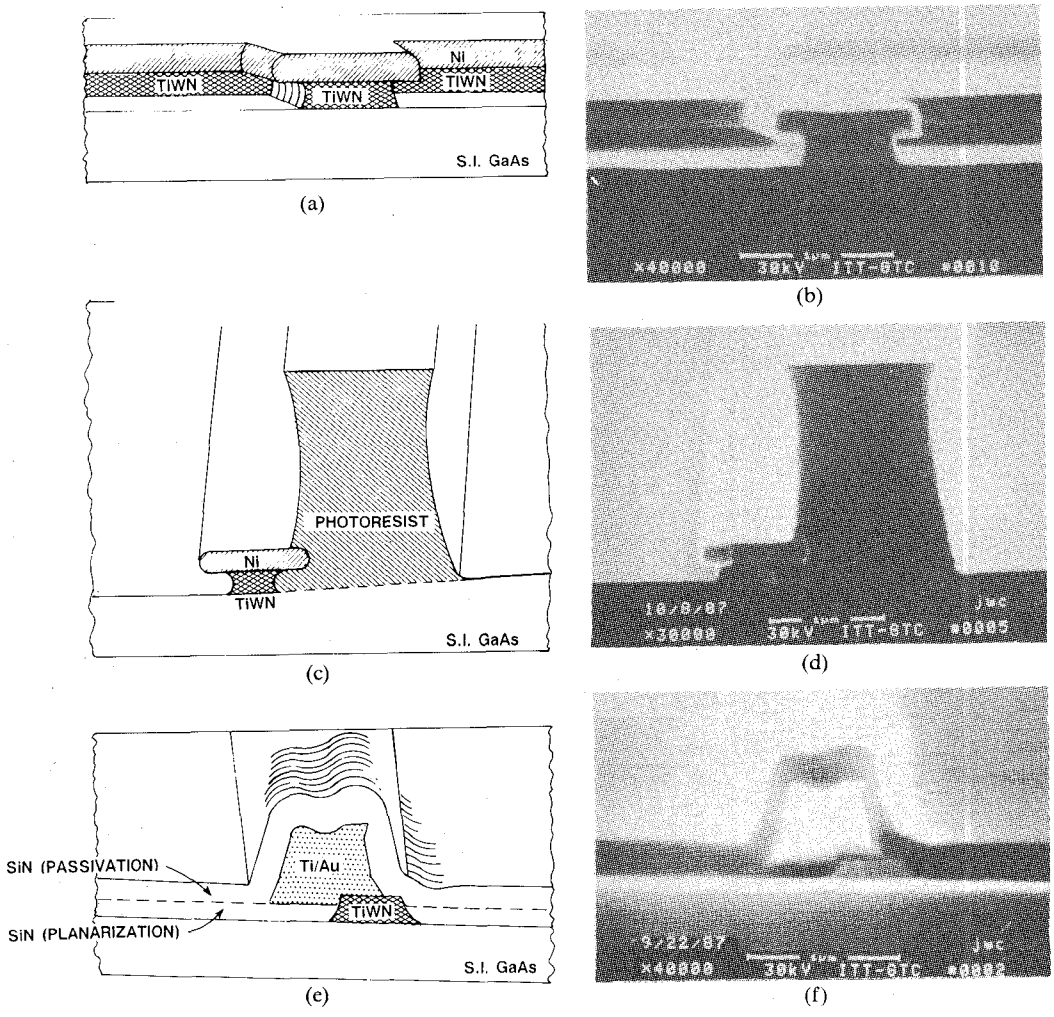


Fig. 2. (a) Sketch and (b) SEM of the symmetric T gate used for the digital FET n+ implant. (c) Sketch and (d) SEM of the asymmetric structure used for the microwave FET n+ implant. (e) Sketch and (f) SEM of the final gate electrode showing overlay metal and passivation.

the amplifier have diode limiters which restrict the maximum signal amplitude.

The circuit operates from +5 V and −5.2 V power supplies with three dc bias connections (one gate and two drain). The drain bias pads are located on the top edge of the chip; the gate bias pads are located on the bottom edge of the chip (see Fig. 3(c)). Every FET is designed to be operated at 10 mA; therefore, the IC will use a maximum current of 60 mA. The drain pads are separated to prevent the likelihood of RF feedback through the bias distribution network.

The limiting amplifier circuit contains two variable resistors to adjust the gate biases. Since the power supplies for the circuit are fixed at +5 V for the drain supply and −5.2 V for the gate supply, it is sometimes necessary to adjust the gate bias to compensate for process variations. The first variable resistor can be adjusted to give the proper gate-to-source voltage (approximately −0.7 V) for the first stage, which controls the input *VSWR*. The second variable resistor can be adjusted to give the proper gate-to-source voltage for stages two through six. The second resistor controls the overall amplifier gain. Typically, the resistors need no adjustment, and no resistor trimming was employed to obtain the results reported here.

The circuit has been designed to be wafer tested with RF probes from Cascade Microtech, Inc. The outside edges of the chip contain a ground bus to allow the RF probes to be used. In addition, RF probe pads are placed on the perimeter of the chip to allow RF probing of individual amplifier stages.

Fig. 4 summarizes the performance of the limiting amplifier. This figure also shows the measured gain of the limiting amplifier at various temperatures. In addition, the measured noise figure and *VSWR* were less than 5 dB and 2, respectively, over the 0.2 to 2 GHz frequency range. The lot-averaged yield of the amplifier as a separate chip is 72 percent of the dc-good chips (43 percent total yield), where the RF-pass criterion is a 1.5 dB gain flatness window about the wafer-averaged gain across the 0.2 to 2.0 GHz frequency band.

B. Prescaler

The dual-modulus prescaler (Fig. 3(b)) has been designed using edge-triggered D-type flip-flops with five gate delays. The prescaler is programmed to divide by 10 or 11

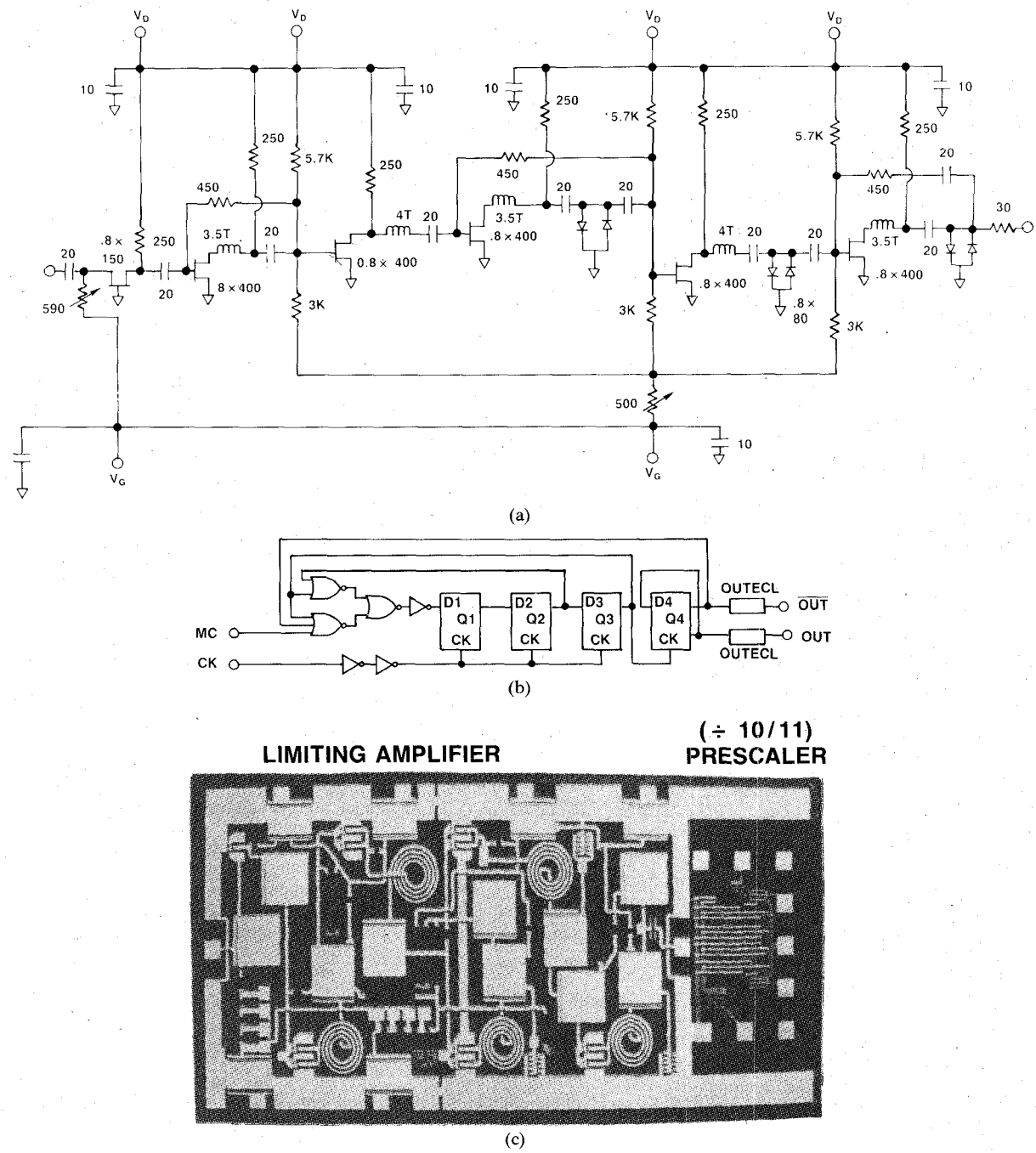


Fig. 3. (a) Schematic of the limiting amplifier, (b) logic schematic of the prescaler, and (c) SEM of the buffered prescaler chip. The chip size is 1.7 mm × 3.7 mm.

and its division is controlled by the mode-control (MC) input. The input to the prescaler is from the output of the limiting amplifier, which is 0 to 0.8 V. The mode-control input and the prescaler outputs are ECL compatible. Two prescaler outputs, Q and Q_b, are available. The prescaler was designed to operate from the 5.0 V and −5.2 V power supplies required by the limiting amplifier, and was implemented in GaAs E/D direct-coupled FET logic (DCFL).

The dual-modulus prescaler was tested on wafers using high-frequency probe cards. Table I presents the high-frequency performance and yield for the separate prescaler chips from wafer number two and wafer number three of the lot. As shown in the table, the DCFL dual-modulus (÷10/11) prescalers were tested to 2.5 GHz, and the average yield was 80 percent.

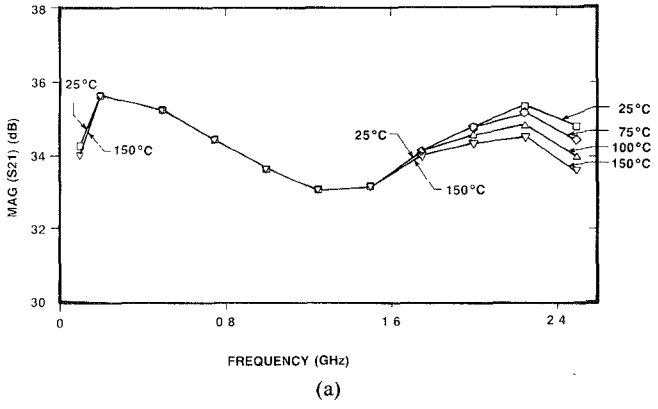
The performance of the prescaler as a function of temperature has also been characterized. Packaged circuits were functionally tested while being heated on a temperature-controlled stage. We observed a nominal decrease of 7 to 10 percent in maximum frequency of operation when the circuits were tested from room temperature to 125°C (Fig. 5). We obtained nearly identical results from several chips, and no hysteresis was observed with rising or falling temperature.

C. Buffered Prescaler

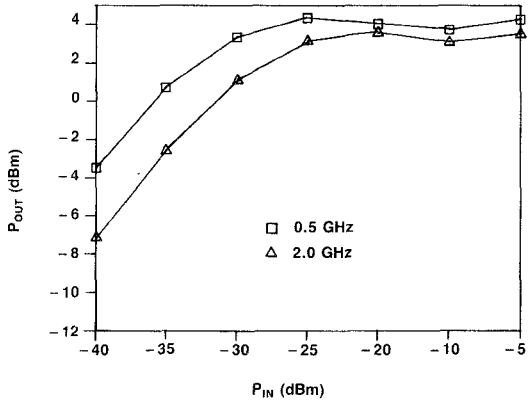
Fig. 6 shows the maximum frequency of the monolithically integrated limiting amplifier/prescaler chip versus

TABLE I
DUAL-MODULUS (−10/11) PRESCALER PERFORMANCE AND YIELD

	Wafer #2		Wafer #3	
	Mean	Best	Mean	Best
Power dissipation (mW)				
w/o drivers	131	143	125	124
w/drivers	208	219	203	199
Max. frequency (GHz)	2.12	2.52	1.73	2.06
Yield	77%	—	83%	—



(a)



(b)

Fig. 4. (a) Limiting amplifier chip gain (*MAG* of *S*21) as a function of frequency at various temperatures with input power = −30 dBm. (b) Output power as a function of input power at two frequencies.

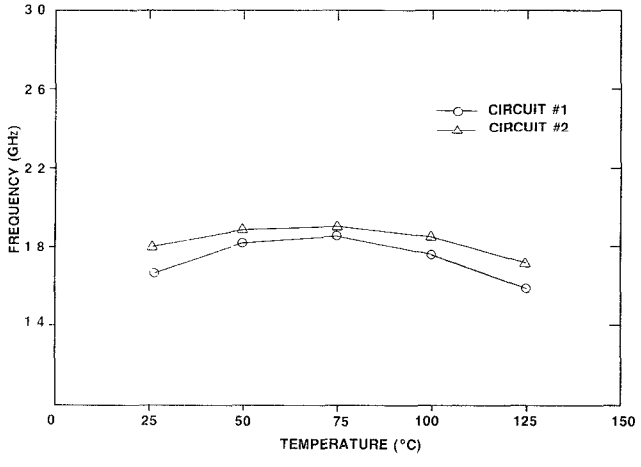


Fig. 5. Dual-modulus (÷10/11) prescaler maximum operating frequency versus temperature.

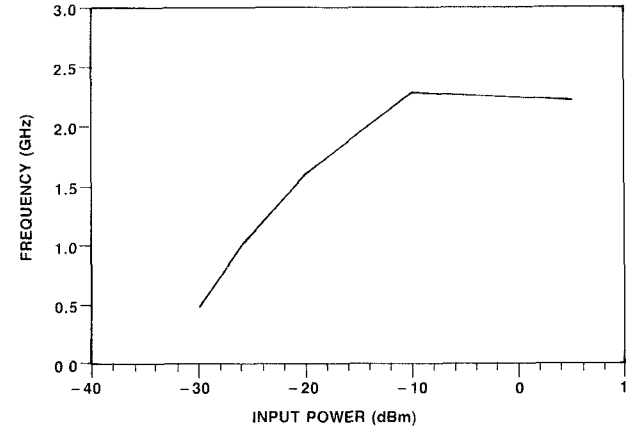


Fig. 6. Maximum output frequency of the buffered prescaler versus input power.

TABLE II
INTEGRATED BUFFER AMPLIFIER/PRESCALER CIRCUIT PERFORMANCE AND YIELD

	WAFER # 1		WAFER # 2		WAFER # 3	
	MEAN	BEST	MEAN	BEST	MEAN	BEST
Power Dissipation						
Prescaler (mW)	130	128	140	154	133	130
Buffer Amplifiers (mW)	487	479	487	503	447	430
Total (mW) (incl. output drivers)	701	690	717	751	671	645
Frequency (GHz)	1.44	1.75	1 41	1.77	1 51	1.93
Yield	9/35 25%	----	16/35 45%	----	14/35 40%	----

(Circuit Test with −22 dBm Input Signal Power)

input power. For inputs from −22 dBm, all RF-good chips were fully functional up to 1 GHz. In addition, while the buffered prescaler circuit was not designed to have a specified noise immunity, it is characterized for noise immunity at various combinations of signal and noise frequencies and power levels. The results are presented graphically in Fig. 7.

Table II presents statistical RF performance and yield data of the buffered prescaler chips from the three dc-good wafers in the lot. All measurements were made with a specified −22 dBm input signal power. Under these test

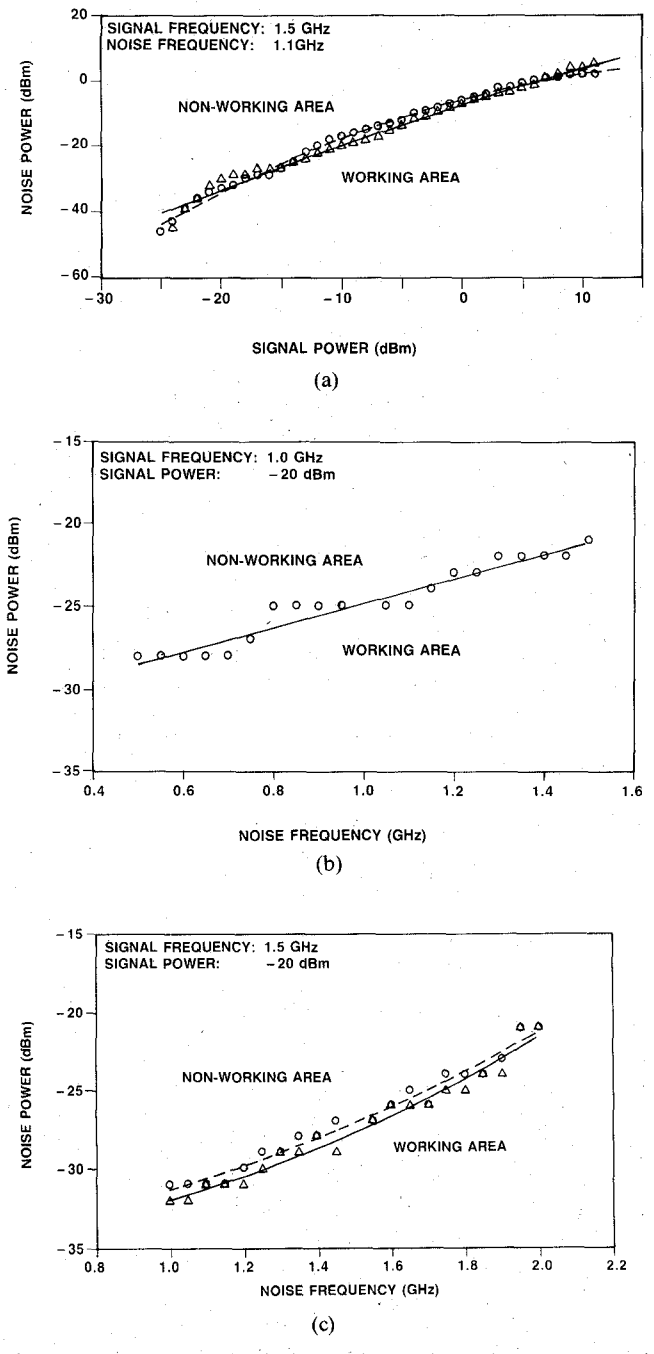


Fig. 7. Effect of noise on the buffered prescaler performance. (a) Noise power required for incorrect circuit performance as a function of signal power at fixed signal and noise frequencies. (b) Noise power required for incorrect circuit performance as a function of noise frequency at a fixed signal power of −20 dBm and a frequency of 1.0 GHz. (c) Same as (b) but at a signal frequency of 1.5 GHz.

conditions, the three wafers described in Table II have an average maximum operating frequency of 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW). Since the average RF yield of the three wafers was 37 percent and the wafer yield from processing was 50 percent (3 of 6), the total lot RF yield was 19 percent. This yield is unexpectedly high considering that: 1) it is our first attempt to fabricate a monolithically integrated analog and digital circuit; and 2) the circuit is highly integrated, containing six microwave FET's, six diodes, five spiral inductors, 16 metal–insulator–metal capacitors, 26 resistors, and 35 digital logic gates. We attribute the high yield to the excellent uniformity and process simplicity inherent in refractory SAG technology.

IV. Summary

A refractory self-aligned gate technology for producing fully planar monolithically integrated analog and digital integrated circuits is demonstrated by fabricating a combined analog and digital chip. We present processing details, circuit design, RF performance, and yield data for an ECL-compatible, *L*-band, limiting dual-modulus (÷10/11) prescaler. When tested with −22 dBm input signal power, one lot of six wafers had a total RF chip yield of 19 percent (39 out of 210) with a best-wafer yield of 43 percent. The average operating frequency is 1.45 GHz (SD = 51 MHz) with an average power dissipation of 696 mW (SD = 23 mW).

Acknowledgment

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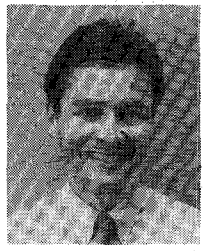
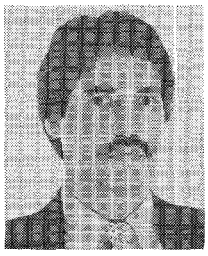


Arthur E. Geissberger (M'84) was awarded the B.S. degree in physics from Lafayette College, Easton, PA, in 1975. In 1976 and 1981 he received, respectively, the M.S. and Ph.D. degrees in solid-state physics from Brown University, Providence, RI.

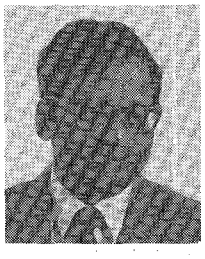
From 1981 to 1983 he was a member of the opto-electronics group at the Xerox Corporation, Palo Alto Research Center, Palo Alto, CA. There he was responsible for fabrication and structural investigation using Raman spectroscopy of bulk and thin-film oxide glasses. He joined the ITT-Gallium Arsenide Technology Center, Roanoke, VA, in August 1983. In his current position, he is responsible for advanced device and process development in the area of microwave and digital self-aligned gate GaAs integrated circuits.



Robert A. Sadler (S'76–M'84) was born at Fort Campbell, KY, on February 1, 1954. He received the B.S. and M.S. degrees in electrical engineering from North Carolina State University, Raleigh, in 1978 and 1980, respectively, and the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, in 1984. His doctoral research was on submicrometer-gate self-aligned GaAs MESFET's for digital IC's.

While at Cornell, he was a Howard Hughes Doctoral Fellow at the Hughes Research Laboratories, Malibu, CA, where he worked on electron-beam lithography and the early development of refractory self-aligned gate fabrication technology. In 1984, he joined the ITT Gallium Arsenide Technology Center, Roanoke, Va, with responsibility for GaAs materials and selective ion implantation process development. His present responsibilities include digital IC fabrication and the development of advanced devices, particularly heterostructure FET's.

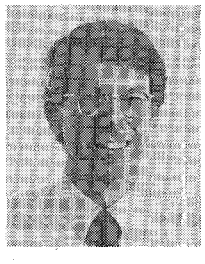
Dr. Sadler is a member of the American Vacuum Society and has authored or coauthored more than 30 technical papers on GaAs materials and devices.



Hausila P. Singh (M'81–SM'88) was born in Varanasi, India, in 1942. He received the B.S. degree (with honors), the M.S. degree in physics, and the Ph.D. degree in solid-state physics from the Banaras Hindu University, India, in 1963, 1965, and 1968, respectively.

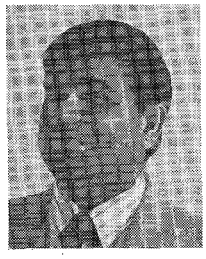
He was with the Birla Institute of Technology and Science, Pilana, India, from 1968 to 1969, where he taught courses in physics. He was a Postdoctoral Research Fellow at the Massachusetts Institute of Technology, Cambridge, and at the University of Southern California, Los Angeles, from 1969 to 1972. He spent six years as a Reader in Physics at Punjabi University, India, where he taught graduate courses in solid-state physics and was engaged in research on the electrical properties of metal–insulator and metal–semiconductor devices. From 1978 to 1982, he was associated with Wright Patterson Air Force Base, Dayton, OH, as a Senior Visiting Scientist, where he was involved in the research and development of high-speed digital circuits utilizing GaAs insulated-gate FET's. He joined the ITT Gallium Arsenide Technology Center, Roanoke, VA, in 1982 as Senior Principal Scientist. In his current position as Technical Staff Fellow, he is responsible for the design and testing of high-speed GaAs digital circuits. He is the author or coauthor of more than 75 research papers and technical reports.

Dr. Singh was awarded a Certificate of Recognition by the Electron Microscopy Society of America in 1972 for Best Physical Science Application: "An Electron Microscope Study of Vapor-Liquid-Solid Growth in In and Sn Thin Films."



Gary K. Lewis (M'87) was awarded the B.S. degree in electrical engineering from the University of Arizona in 1977, and the M.S.E.E. degree in 1981 from the California State Polytechnic University.

He joined the ITT Gallium Arsenide Technology Center, Roanoke, Va, in 1985 after seven years on the technical staffs of General Dynamic's Pomona Division and Litton System's Amecom Division. At those companies, he developed microwave frequency synthesizers and microwave receiver subsystems. He also spent three years on the technical staff at the Navy's Fleet Analysis Center and the Air Force's Chanute Technical Training Center, certifying missile test systems and teaching aircraft repair.



Inder J. Bahl (M'80–SM'80) was born in India in 1944. He received the M.S. degree in physics and the M.S. degree in electronics engineering from the Birla Institute of Technology and Science, Pilani, India, in 1967 and 1969, respectively, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology (IIT), Kanpur, India, in 1975.

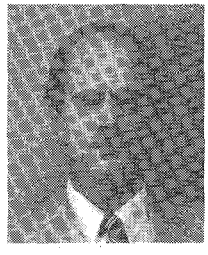
From 1969 to 1974, he was a Senior Research Assistant at IIT Kanpur. From 1974 to 1978, he was with the Advanced Centre for Electronic Systems as a Research Engineer, where he was engaged in research on p-i-n diode phase shifters, microwave integrated circuits, and printed antennas. From 1979 to 1981, he was a Research Associate at the University of Ottawa, Canada. Prior to joining ITT in 1981, he spent five months at the Defense Research Establishment, Ottawa, Canada, working on millimeter-wave systems as a Research Scientist. At ITT GTC, in his present capacity as a Technical Staff Fellow, he is responsible for the design of GaAs analog IC's, testing of IC's, and operation of the hybrid facility.

Dr. Bahl is the author or coauthor of over 100 research papers and technical reports. He has coauthored four books: *Microstrip Lines and Slotlines* (Artech House), *Microstrip Antennas* (Artech House), *Millimeter Wave Engineering and Applications* (Wiley), and *Microwave Solid State Circuit Design* (Wiley). He holds five patents in the areas of microstrip antennas and microwave circuits.

Matthew L. Balzan (S'80–M'86) was born in Chattanooga, TN, in 1960. He attended the University of Virginia in Charlottesville, where he received the B.S. degree in electrical engineering in 1983. He is presently an M.S. candidate there, also in electrical engineering.

While in Charlottesville, he worked for the General Electric Company Industrial Electronics Development Laboratory in the area of semicustom IC design. In 1985 he joined the ITT Gallium Arsenide Technology Center Roanoke, VA. There his responsibilities have included process and device development for self-aligned gate FET's in microwave, digital, and switching applications.

Mr. Balzan is a member of Tau Beta Pi, Eta Kappa Nu, and the American Vacuum Society.

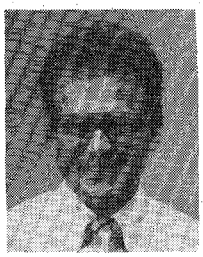


Edward L. Griffin (M'76) was born in Philadelphia, PA, in 1947. He obtained the B.S. degree in engineering physics in 1969, the M.S. degree in physics in 1971, and the Ph.D. degree in solid-state physics in 1975, all from the University of Illinois.

He has over 13 years of microwave and high-speed digital experience. He worked for seven years at Hughes Aircraft Company Space and Communications Group (SCG). Areas of specialty included microwave filters and GaAs FET

power and low-noise amplifiers for space applications. Dr. Griffin joined ITT Electro Optical Products Division in 1982 as Manager of GaAs IC Design and Test. In 1985, he became Manager of GaAs IC Fabrication, ITT Gallium Arsenide Technology Center (ITT-GTC), and in 1986, Director of Engineering, ITT-GTC, Roanoke, VA.

Dr. Griffin served on the IEEE MTT Microwave Filter Steering Committee from 1981 to 1983 and the IEEE MTT Low Noise Techniques Technical Committee in 1985. He is the author or coauthor of more than 11 technical papers and is the coholder of eight microwave patents. Dr. Griffin is a member of the American Physical Society.



Monte J. Drinkwine (M'86) received the B.S. and M.S. degrees from the University of Milwaukee in 1970 and 1975, respectively. In 1977 he received the Ph.D. degree in physics, also from the University of Milwaukee.

From 1979 to 1983 he worked for ITT in developing a production-worthy generation III image intensifier technology based on MOCVD-grown GaAs photocathodes. Since then his efforts have been in the field of GaAs IC process development. He has contributed to the successful development of ITT's multifunction self-aligned gate GaAs IC fabrication process and presently manages ITT-GTC's GaAs IC wafer fabrication effort.